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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,707	10/23/2003	Takio Ohno	67161-122	9729

7590 11/17/2004

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,707	OHNO, TAKIO	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 October 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/23/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 23 October 2003. Claims 1-5 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bullock et al. (2002/0090767) in view of Arai et al. (6,344,384).

Bullock et al. disclose a method of manufacturing a semiconductor device having field effect transistors where a main surface of a silicon substrate (1) has first and second active areas (10b, 10a); forming a first insulating film (22b/22a) on the first and second active areas (10b, 10a) (Fig. 1 & 2; para. 15-16); selectively removing a prescribed portion of the first insulating film (22a) to expose the second active area (10a) (Fig. 4 & 6; para. 17, 19); forming a second insulating film (24b/24a) on the first and second active areas (10b, 10a); performing an annealing process on the first and second insulating films (22a, 24b/24a) at or above a temperature for forming the second insulating film (24b/24a); and forming a first gate electrode (40) on the first active area (10b) such that the first and second insulating films undergoing the annealing process lie between the first active area and the first gate electrode (40) (Fig. 5; para. 18), and

forming a second gate electrode (50) on the second active area (10a) such that the second insulating film (24b) undergoing the annealing process lies between the second active area and the second gate electrode (Fig. 8; para. 20). Bullock et al. do not disclose a trench isolation film is formed at a main surface of a silicon substrate to form first and second active areas.

Referring to claim 2, Bullock et al. disclose the temperature for forming the second insulating film is at most 1000^{o}C (para. 17).

Referring to claim 5, Bullock et al. disclose performing the annealing process in an atmosphere of an inert gas (para. 17).

Arai et al. disclose a method of manufacturing a semiconductor device having field effect transistors where a trench isolation film (3) is formed at a main surface of a silicon substrate (1) to form at least first and second active areas; forming a first insulating film (3a) on the at least first and second active areas (Fig. 3D; col. 10, lines 29-35); selectively removing a prescribed portion of the first insulating film (3a) to expose the second active area; forming a second insulating film (31) on the at least first and second active areas (Fig. 5H; col. 11, lines 29-34); and forming gate electrodes on the at least first and second active area (Fig. 1; col. 9, lines 53-55).

Referring to claim 3, Arai et al. disclose forming the first insulating film through a thermal oxidization process in a wet atmosphere (col. 10, lines 32-35).

Since Bullock et al. and Arai et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device having field effect transistors, the purpose disclosed by Arai et al. would have been recognized in the pertinent art of

Bullock et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bullock et al. by forming a trench isolation film at a main surface of a silicon substrate as taught by Arai et al. to increase current (col. 5, lines 42-48).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bullock et al. in view of Arai et al. as applied to claim 1 above, and further in view of Gardner et al. (5,783,469).

Bullock et al. in view of Arai et al. disclose the subject matter claimed above except performing the annealing process using a rapid thermal anneal (RTA) method.

Gardner et al. disclose a method of manufacturing a semiconductor device having field effect transistors where a main surface of a silicon substrate (12) has first and second active areas (Fig. 1; col. 4, lines 13-39); forming an insulating film (20) on the first and second active areas; performing an annealing process on the insulating film (20) at or above a temperature for forming the insulating film; and forming a first gate electrode (56) on the first active area, and forming a second gate electrode (58) on the second active area (Fig. 6; col. 5, lines 1-26). Gardner et al. further disclose the annealing process is performed with a rapid thermal anneal (RTA) method (col. 5, lines 27-44).

Since Bullock et al. and Gardner et al. are both from the same field of endeavor, a method of manufacturing a semiconductor device having field effect transistors, the purpose disclosed by Gardner et al. would have been recognized in the pertinent art of Bullock et al. Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to modify Bullock et al. by performing the annealing process using a rapid thermal anneal (RTA) method as taught by Gardner et al. to increase current (col. 2, lines 1-40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ramsbery et al. (6,465,306) disclose a method of manufacturing a semiconductor device having field effect transistors where a main surface of a silicon substrate has first and second active areas; forming a first insulating film on the first and second active areas; selectively removing a prescribed portion of the first insulating film to expose the second active area; forming a second insulating film on the first and second active areas; and forming a first gate electrode on the first active area, and forming a second gate electrode on the second active area.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP